Nanoinnovation 2016 Conference & Exhibition

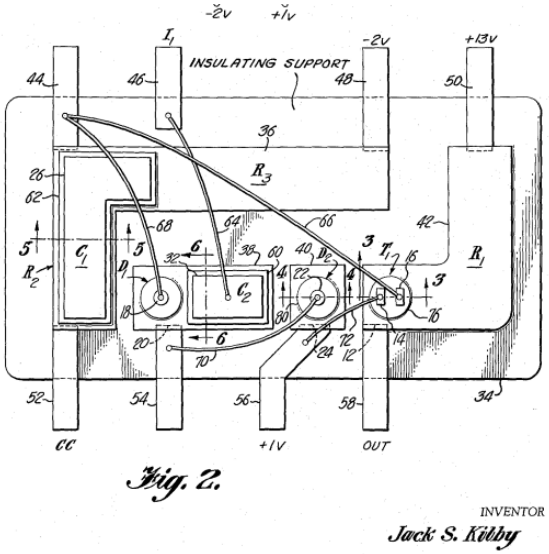
« 3D NAND memory trends »

Senior Director Micron NVE Design Europe

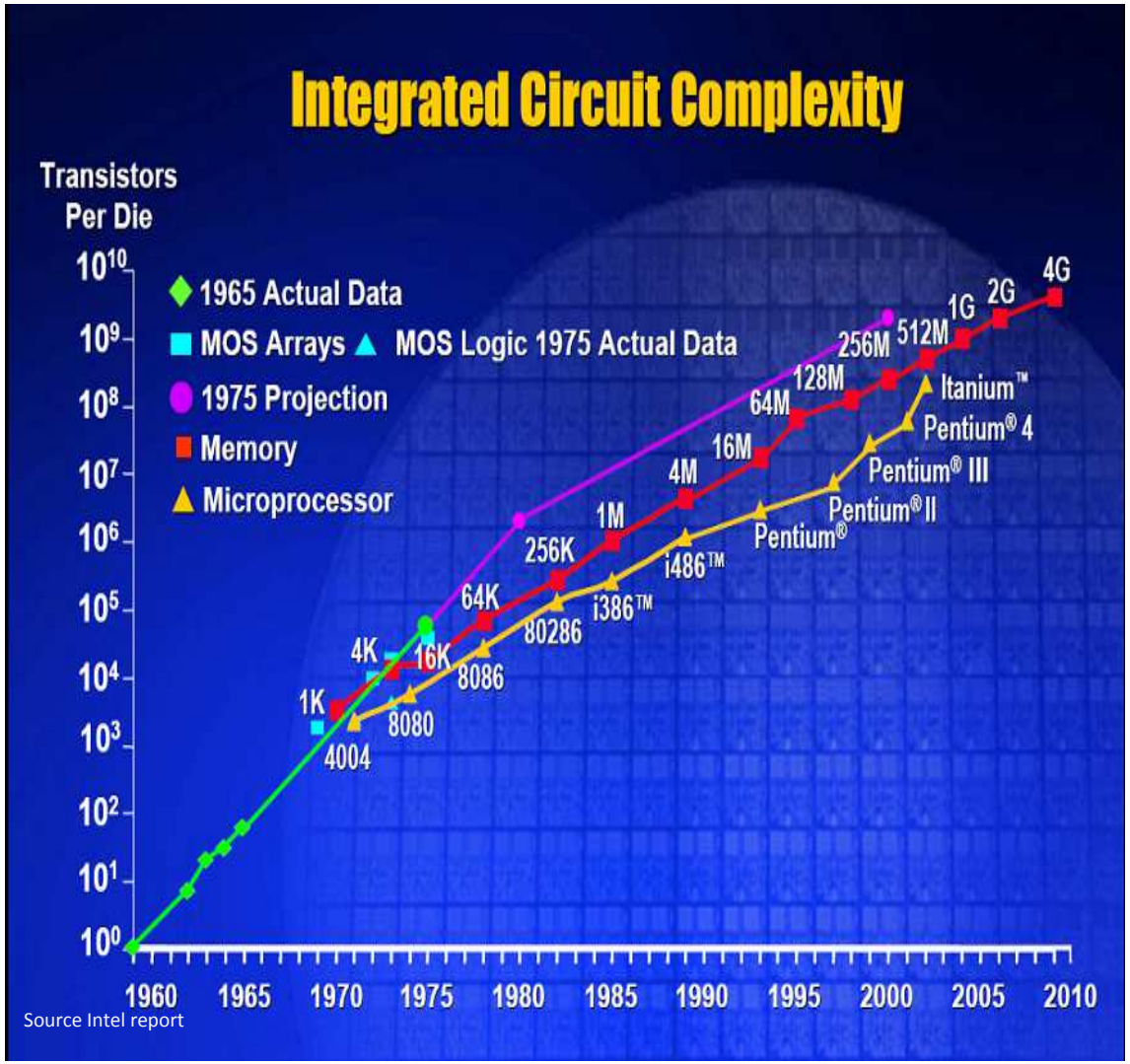
Tommaso Vali

Sept 22

IC (1959)



Moore's law



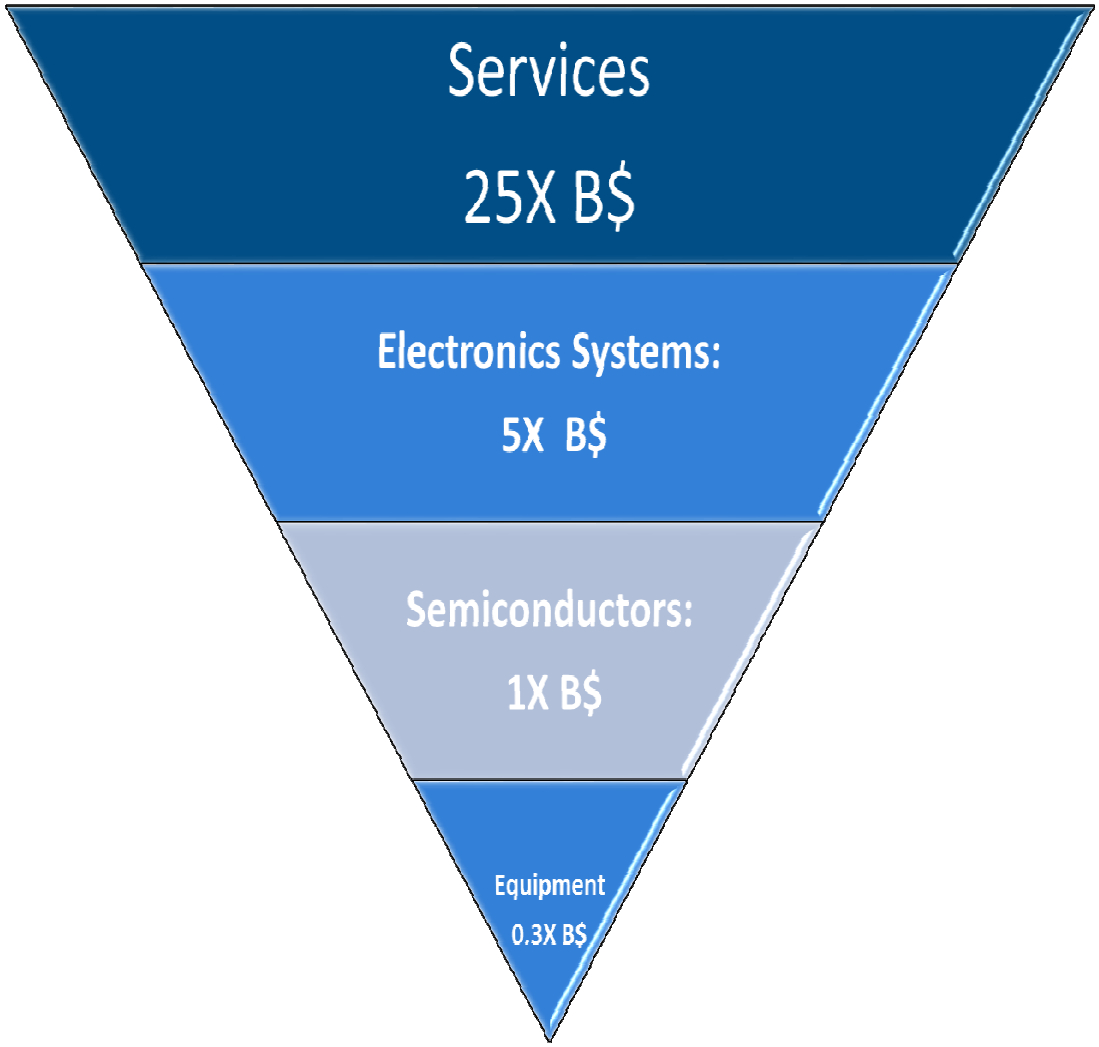
Source Intel report

Semiconductor WW TAM

Spring 2016 Q2 Update	Amounts in US$M				
	2015	2016	2017	2018	2019
Americas	68.738	62.080	62.811	64.112	65.682
Europe	34.258	32.522	32.834	33.457	34.084
Japan	31.102	31.334	32.081	32.592	33.283
Asia Pacific	201.070	198.614	203.274	208.126	212.613
Total World	335.168	324.550	331.000	338.288	345.662
Discrete S/C	18.612	18.995	19.551	20.081	20.568
Optoelectronics	33.256	30.916	31.552	32.642	33.340
Sensors	8.816	10.474	11.198	11.546	11.958
Integrated Circuits	274.484	264.165	268.700	274.018	279.796
Analog	45.228	45.940	47.478	48.833	50.468
Micro	61.298	61.514	62.488	63.567	63.990
Logic	90.753	85.547	84.942	85.882	86.887
Memory	77.205	71.164	73.791	75.737	78.450
Total Products	335.168	324.550	331.000	338.288	345.662

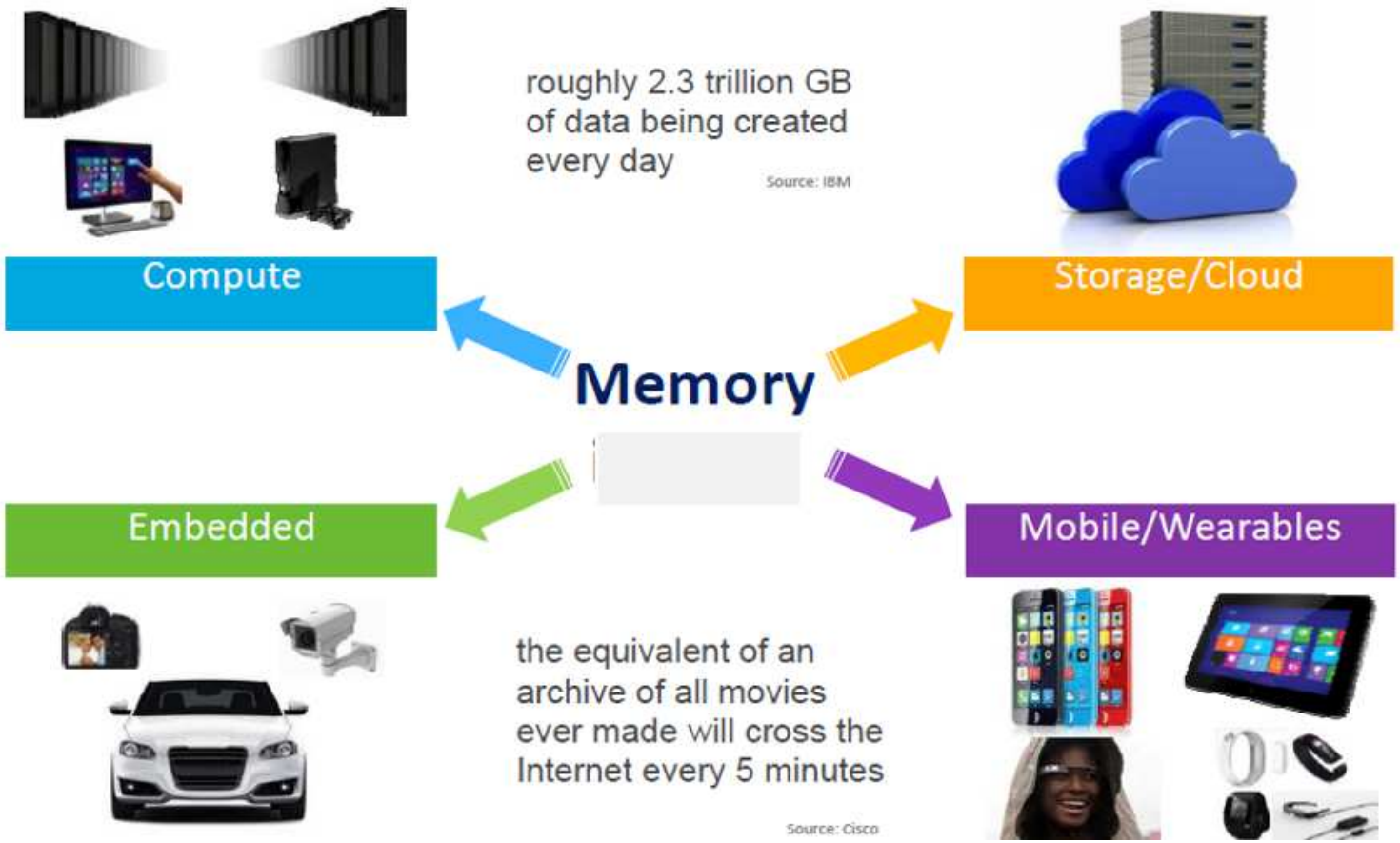
Memory	77.205	71.164	73.791	75.737	78.450
DRAM	44.970	38.172	39.080	39.773	40.526
NOR Flash	1.541	1.604	1.562	1.516	1.500
NAND Flash	28.845	29.647	31.448	32.780	34.787
Total ICs	274.484	264.165	268.700	274.018	279.796

WORLD WIDE Electronic system structure TAM



Source: WSTS

Key Technology Growth Drivers Rely on Memory



MEMORY

DATA : GENERATION-STORAGE-MOBILITY

5 Big technology trends

NETWORKING

MACHINE TO MACHINE

MOBILE

CLOUD

BIG DATA

Semiconductor memories are today a key element of every electronic systems. Advancement in memory technology is feeding the 5 big technology trends which are shaping modern society and human interactions.

Memories: a key element of many electronic systems

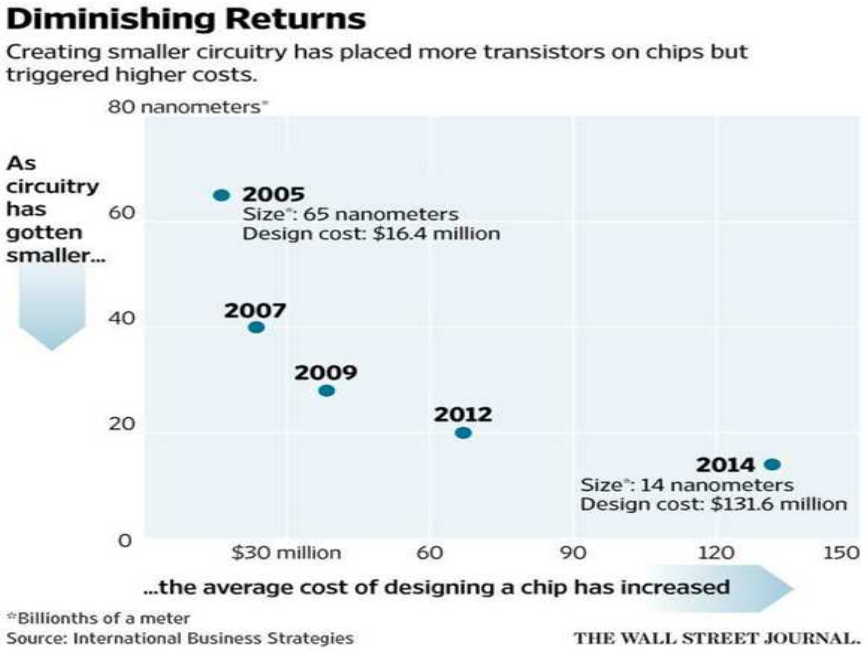
We are used to memories being just a support technology but in last years are becoming increasingly important in defining the overall electronic system.

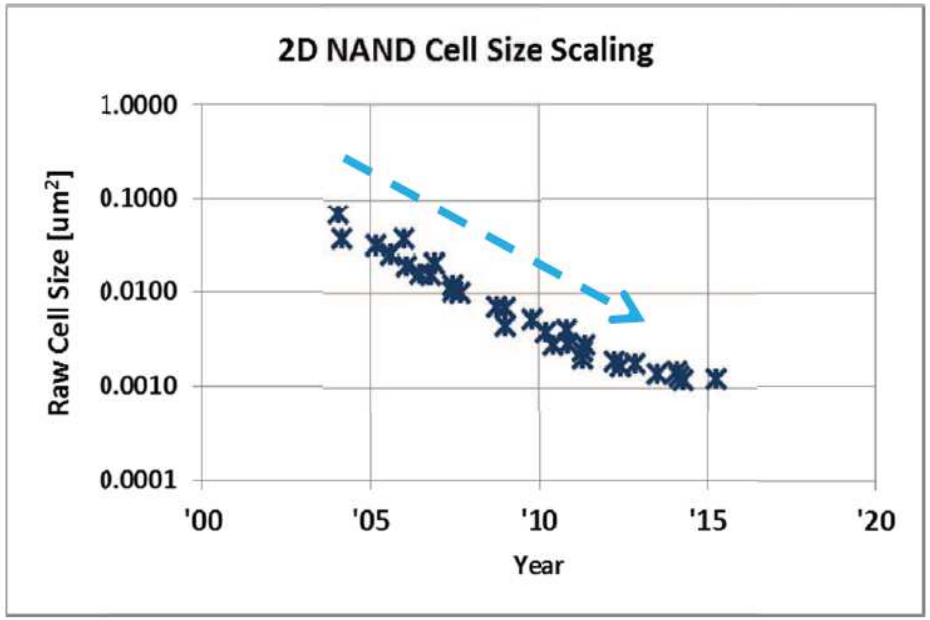
- **SMART PHONE & TABLETS**
  - Memory content cost is higher than the CPU cost
  - Memory density is becoming more often the metric to describe the product performances more than the computational power

- **LAPTOP e SERVERS**
  - Latency and Power are critical parameters just as important as overall computing performances.
    NAND based SSD introduction in computer has significantly improved overall system performances

Scaling Trends

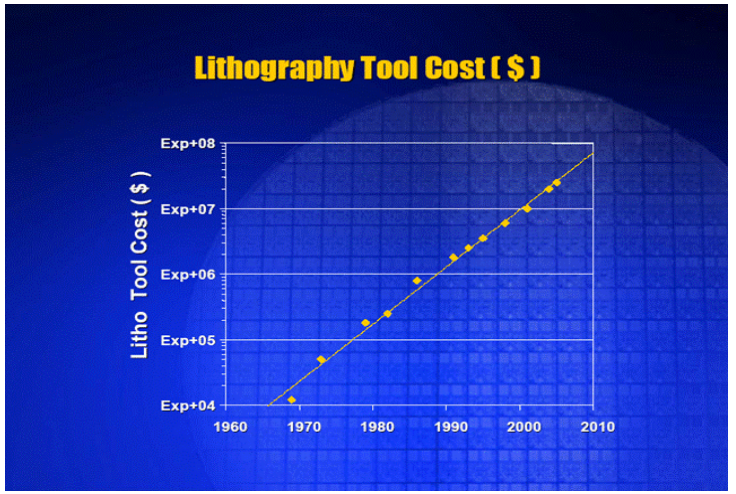
Over the past thirty years , DRAM and then NAND technologies have been able to provide the right products solutions to enable new applications and markets due to the continuous scaling of feature size and performance. Planar NAND has approached in 2010-1015 the sub 20 nm technology range. Scaling beyond current levels is becoming increasingly challenging and costly





CAP FOR A NEW GENERATION MEMORY FAB

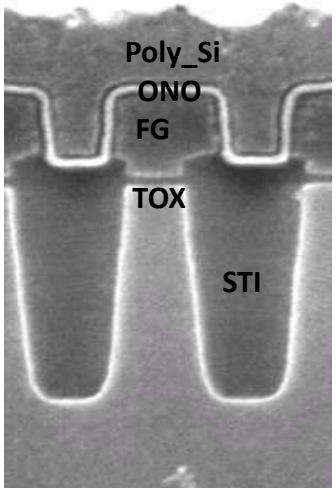
- NAND CAP NEEDED FOR A 100K WPM FAB in SUB 20nm ~4B$
- Equipment cost : lithography tool cost above 50M$

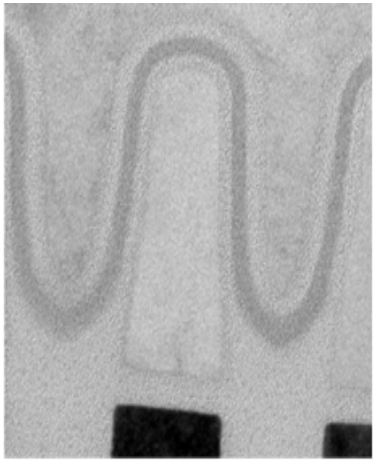


2D NAND

WRAP FLOATING GATE
challenges below 20nm

1) High aspect ratio
2) Fg2Fg Interference
3) E field increase





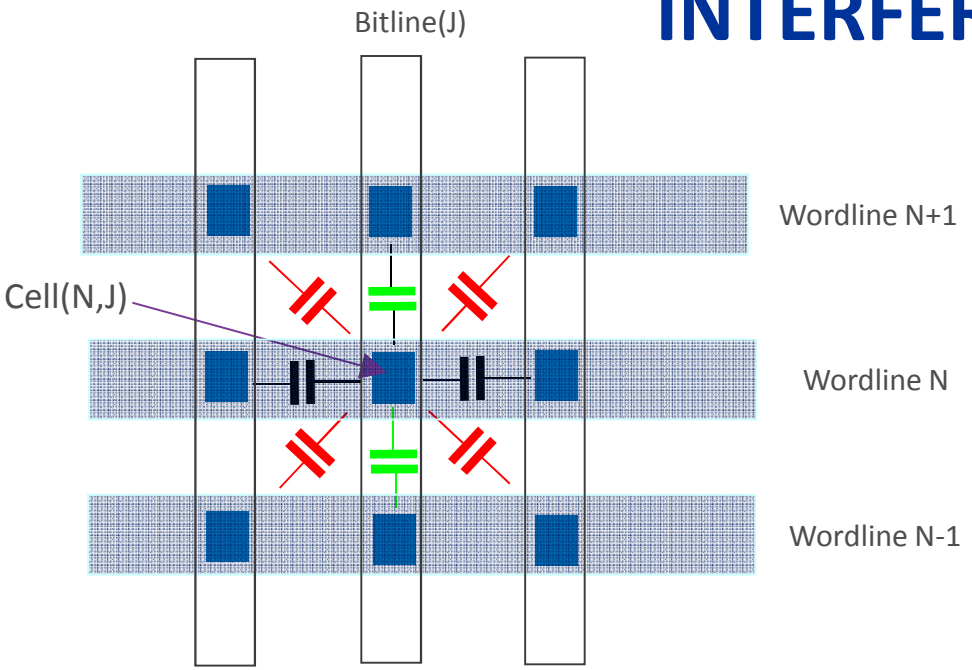
In the conventional WRAP FG cell , interpoly dielectrics IPD and the control gate CG WRAP around the floating gate is used to achieve good coupling ration (GCR)

At 20nm node CG and FG widths become ~10nm . Aspect ratio become >10 in both BL and WL direction.

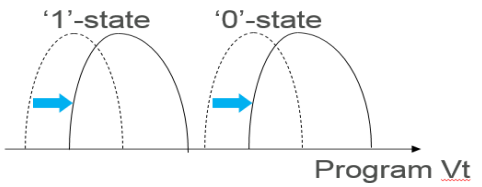
FG height of a wrap FG cell is as tall as >50nm.
Cell to cell interference increases significantly , this widens MLC Vt distributions

Electrical Field at the top of FG and bottom of CG increase with scaling .
This high E filed effects degrade cycling reliability and data retention

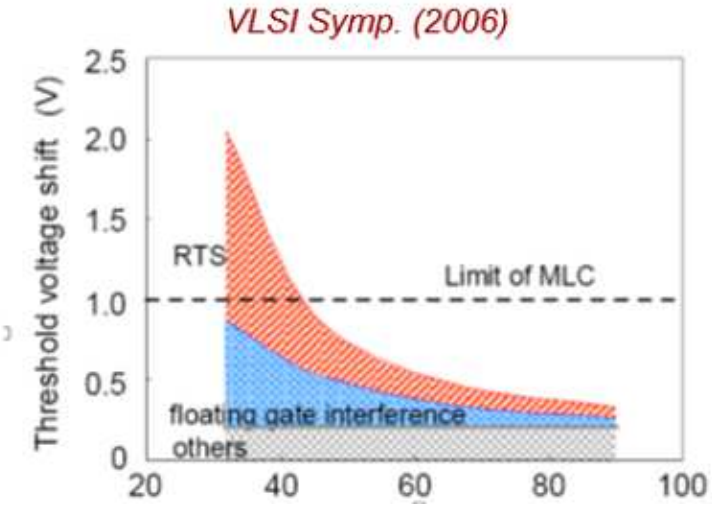
FLOATING GATE TO FLOATING GATE INTERFERENCE



The Floating gate to floating gate interference is the delta Vt induced by capacitor coupling on all surrounding cells when programming a generic cell (N,J)



Program Vt distribution shifts after receiving the coupling noise.



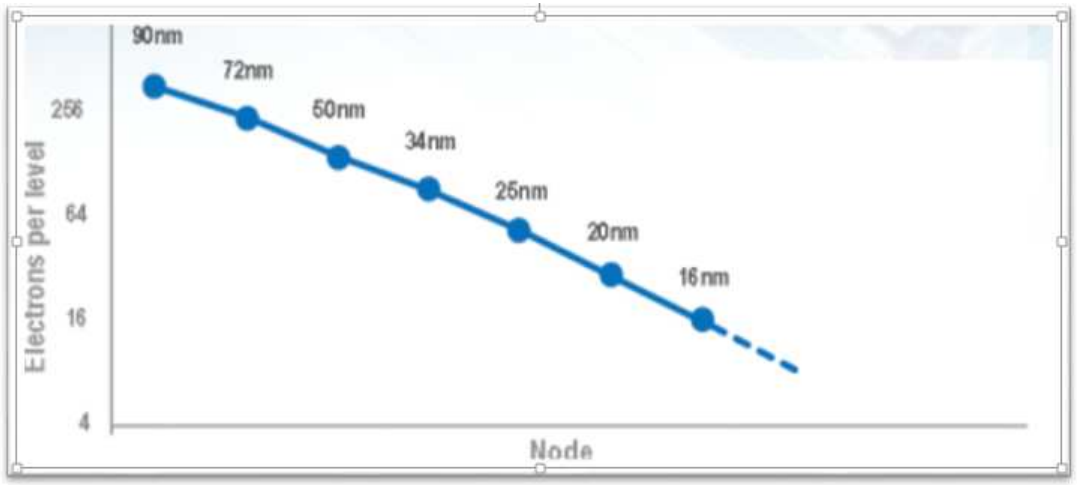
Estimation of threshold voltage shift as a function of process node

Coupling cap along wordlines

Coupling cap along diagonal

Coupling cap along the bitlines

NUMBER OF ELECTRONS



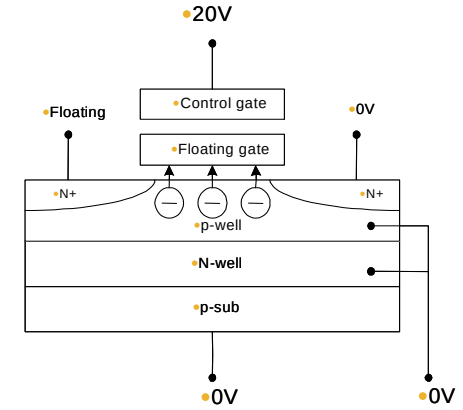
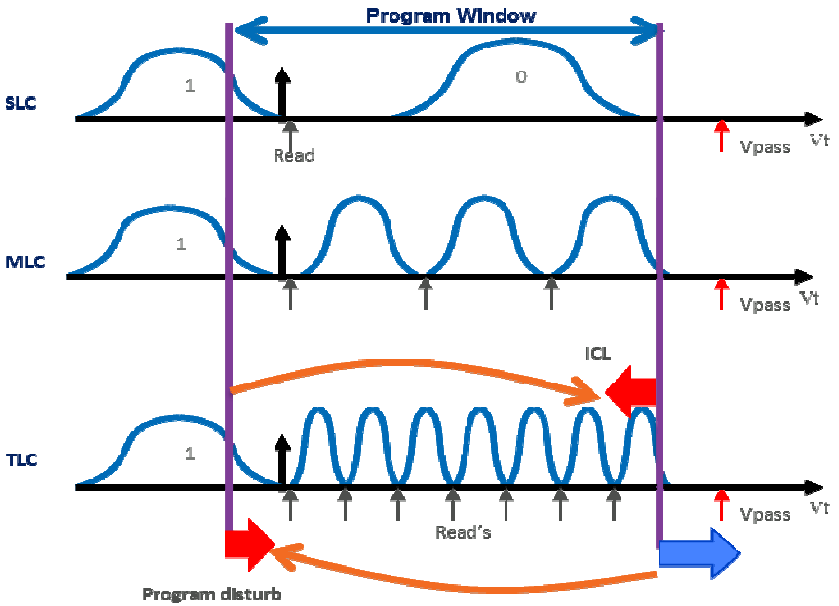


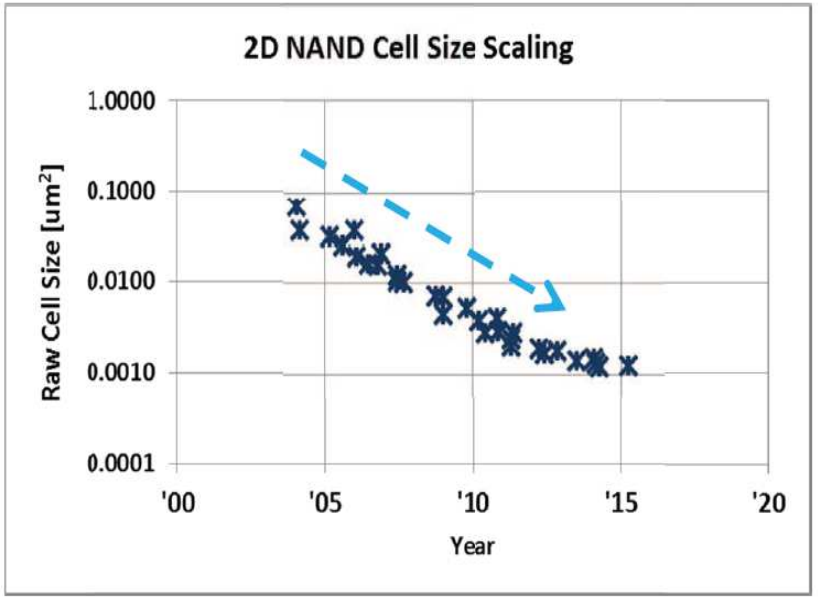
Fig. 3.1 "0" Programming

- Reduced Cell CAP with scaling is reducing # of electrons x state
- States enlargement due to fluctuations effect

2D NAND Flash in last decade

Last decade the physical cell size has shrunk by 100x in area.
Additional cost scaling was achieved by transistionin to **1-2-3bpc**



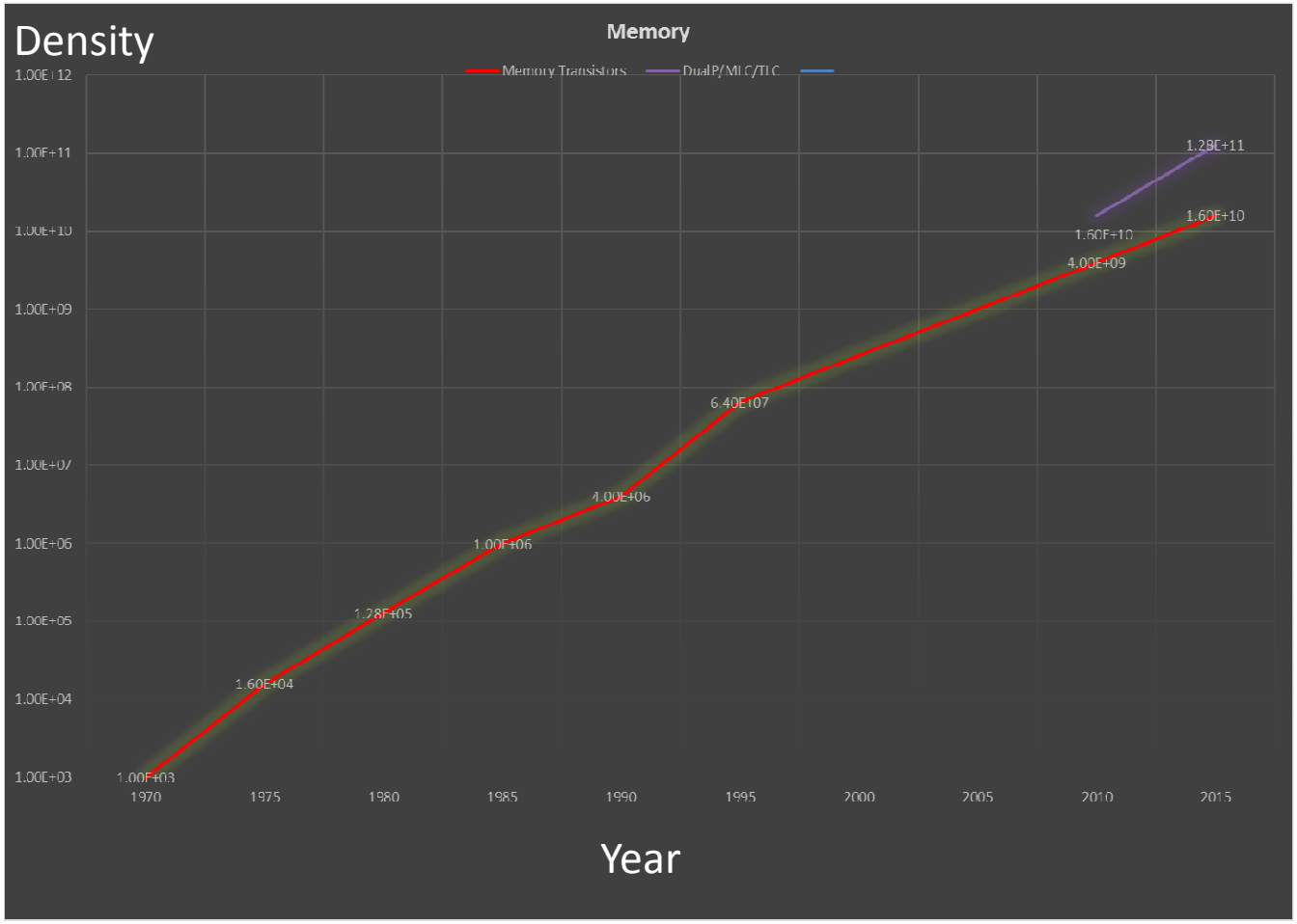


Lithography pitch limits → **Pitch reduction approaches: doubling patterning**

Electrical proximity → **Airgap: WL/STI air gap**

Physical cell scaling → **HiK material Metal gate planar**

“Moore’s law” x Memory



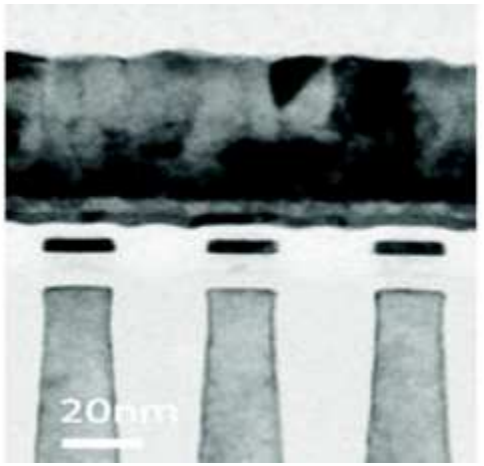
2D NAND Dual Pattening , SLC→MLC→TLC, planar cell

2D NAND

PLANAR FLOATING GATE w/ high K IPD and metal gate

Below 20nm :

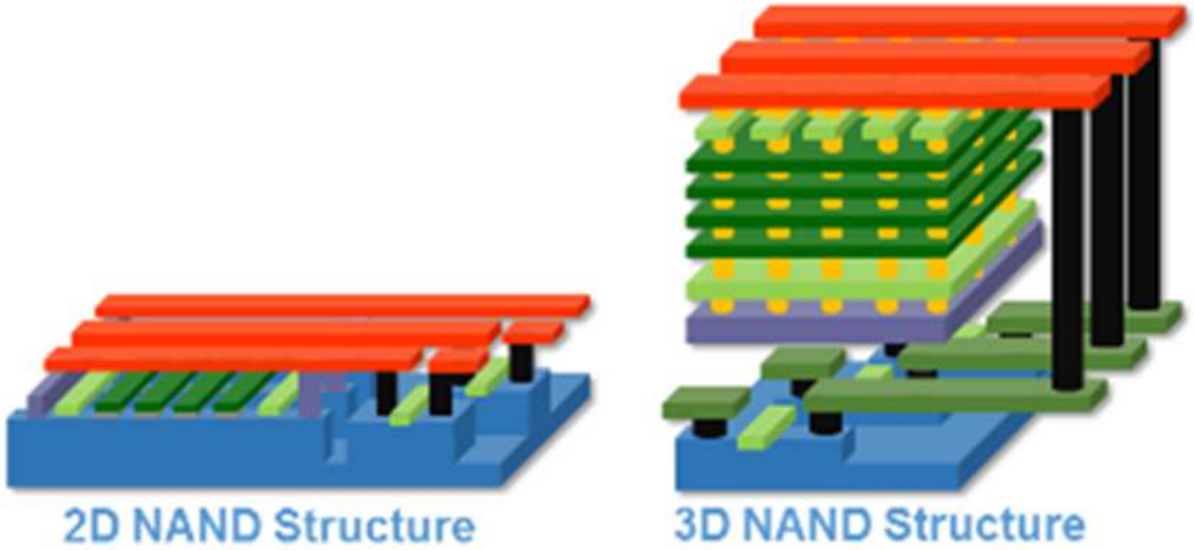
1) Sub 20nm CG and FG width become <10nm
2) Thin charge storage layer (physical scalability)



Thin charge storage layer for physical scalability and low Fg2Fg interference

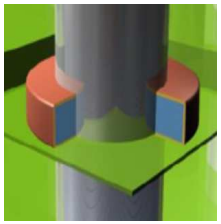
High K is used as blocking dielectric to maintain good gate coupling ratio

3D NAND



3D NAND

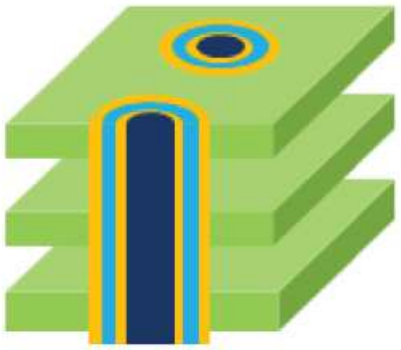
Effective cell scaling is achieved by staking multiple layers. Cell physical cell size is large and this contributes to enhancement cell performances and reliability.



There are 2 types of string architectures:

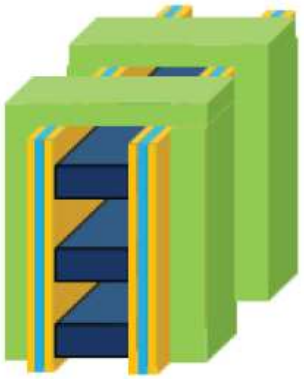
One is **vertical NAND** advantageous in electrical performances and reliability due to the gate all around (GAA)

Vertical channel 3D NAND

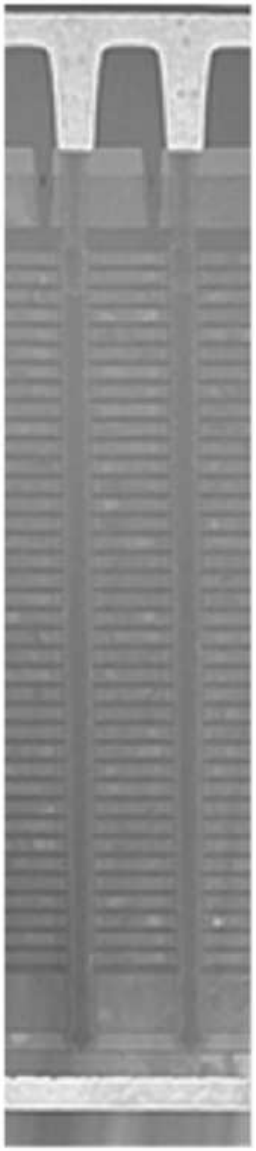


Another option **is Horizontal NAND** : can have smaller cell size due to the smaller physical cell size

Horizontal channel 3D NAND



3D NAND
Micron-Intel



AA conventional floating gate cell was used for its proven reliability.

This first generation of the 3D NAND has 32 Tiers of active wordlines plus additional Tiers for dummy wordlines and source and drain select gates.

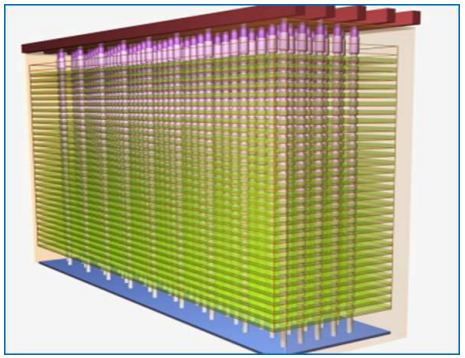
Here a SEM cross-section of the NAND string which is formed completely **above the silicon substrate**.

After the cell hole etch through the wordline tiers, the **control gate is recessed back** and inter poly dielectric is formed.

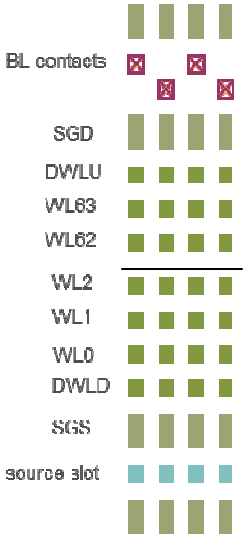
Following this the **floating gate** is deposited and etched back to form isolated floating gate for each cell.

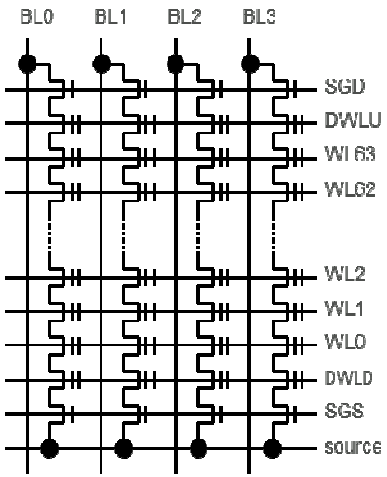
This is followed by the **tunnel-oxide** and channel formation.
While the NAND cells are floating gate cells, the source and drain select devices are single gate oxide transistors.

3-D FG NAND structure

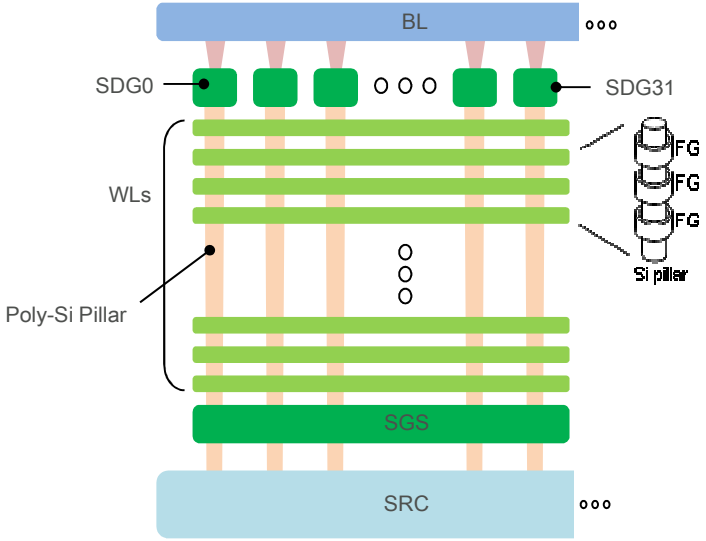


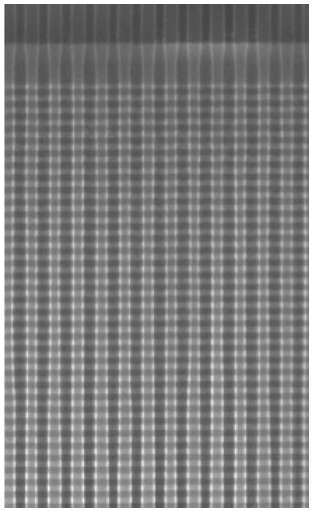
2D NAND STRING



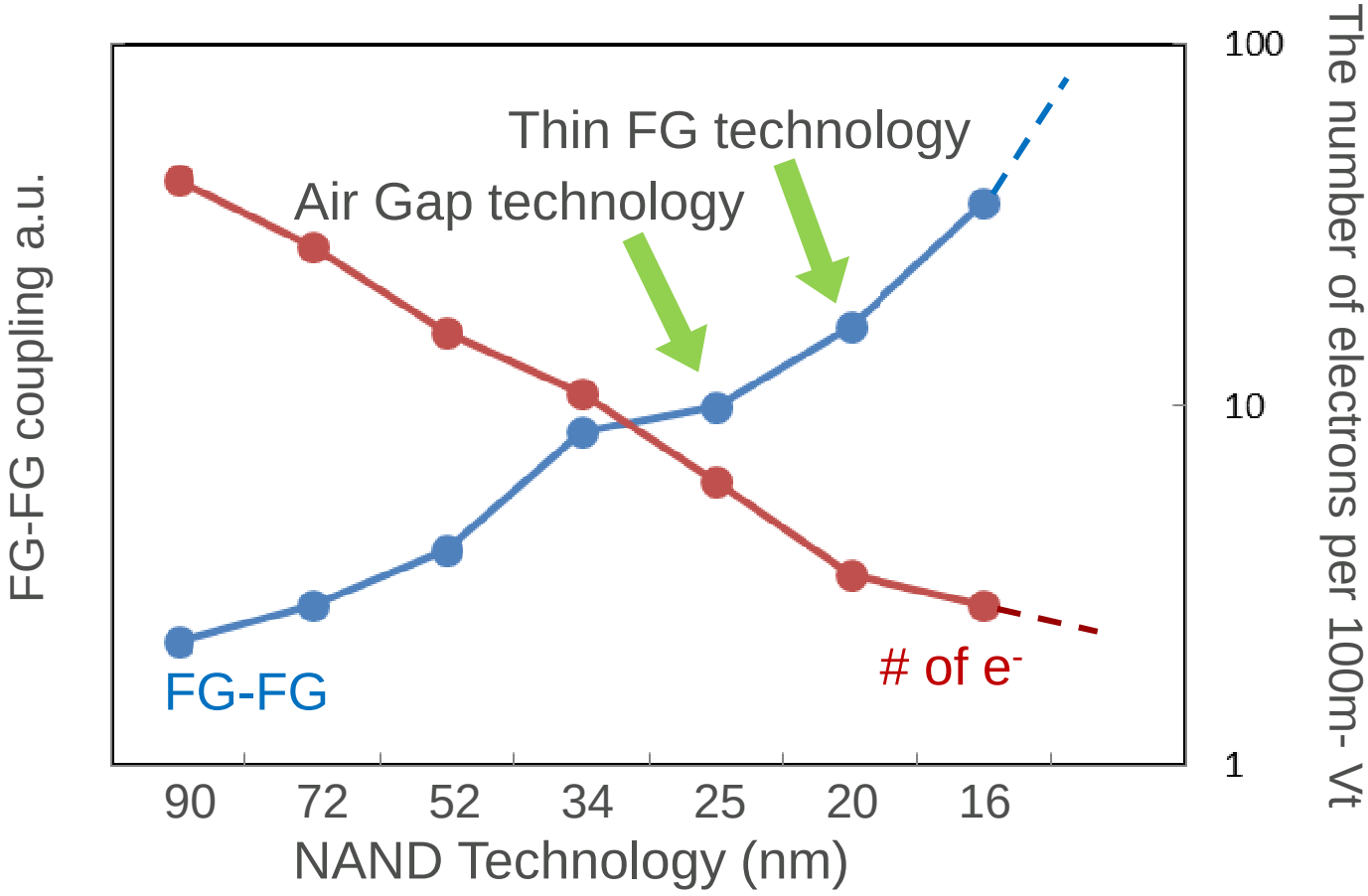


3D NAND STRING



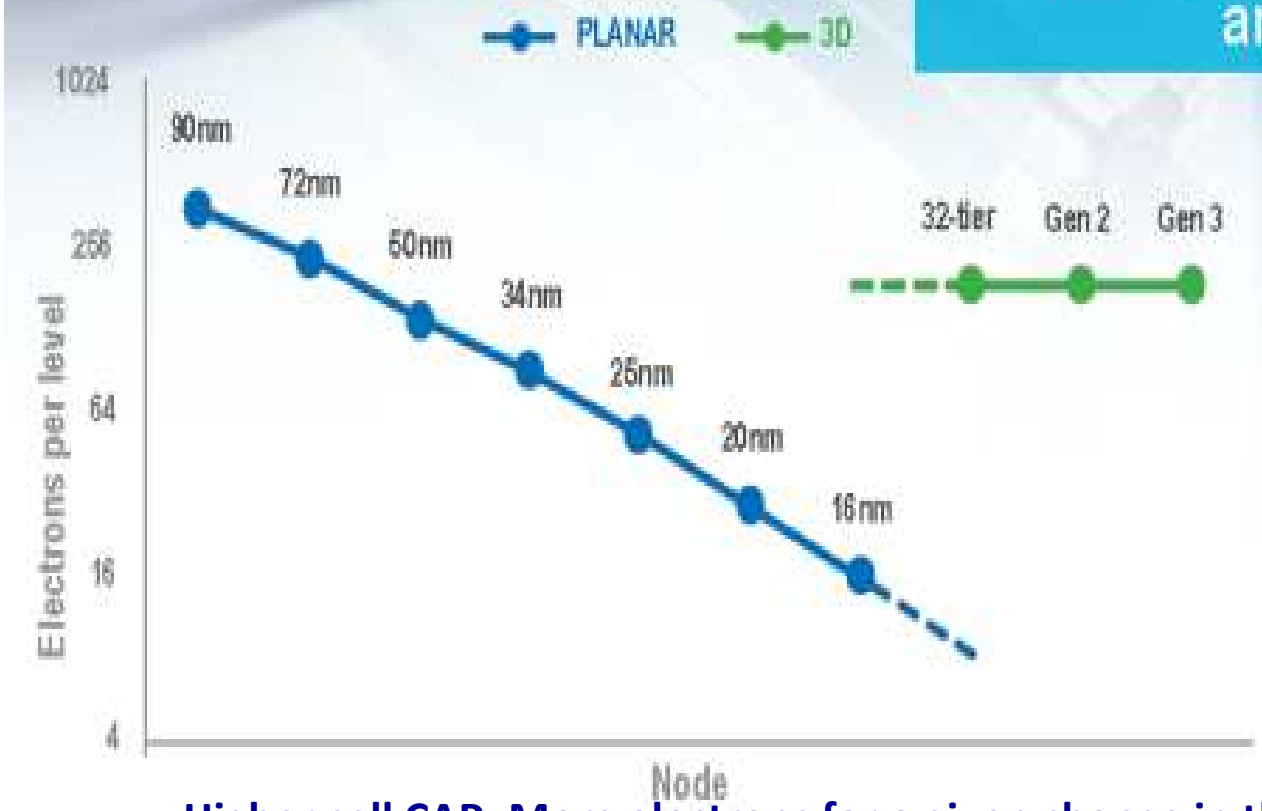


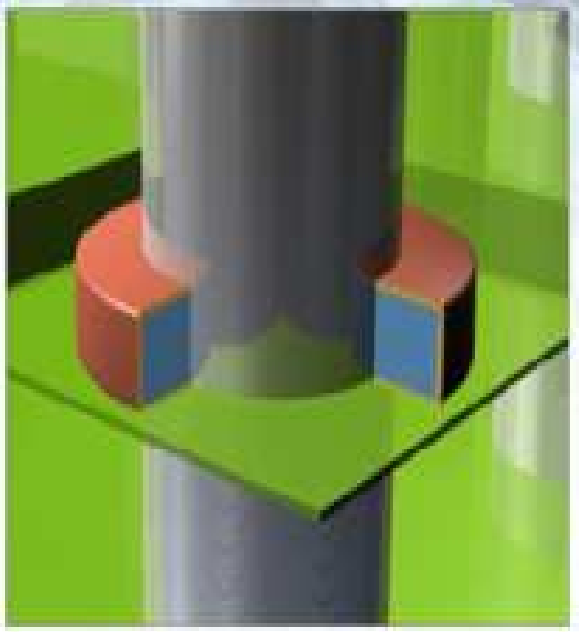
2D FG NAND: ISSUE



Performance and Reliability

Cell design improves performance and reliability

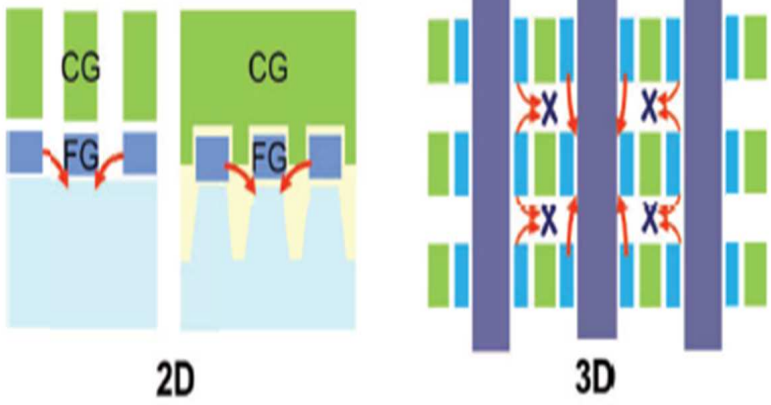


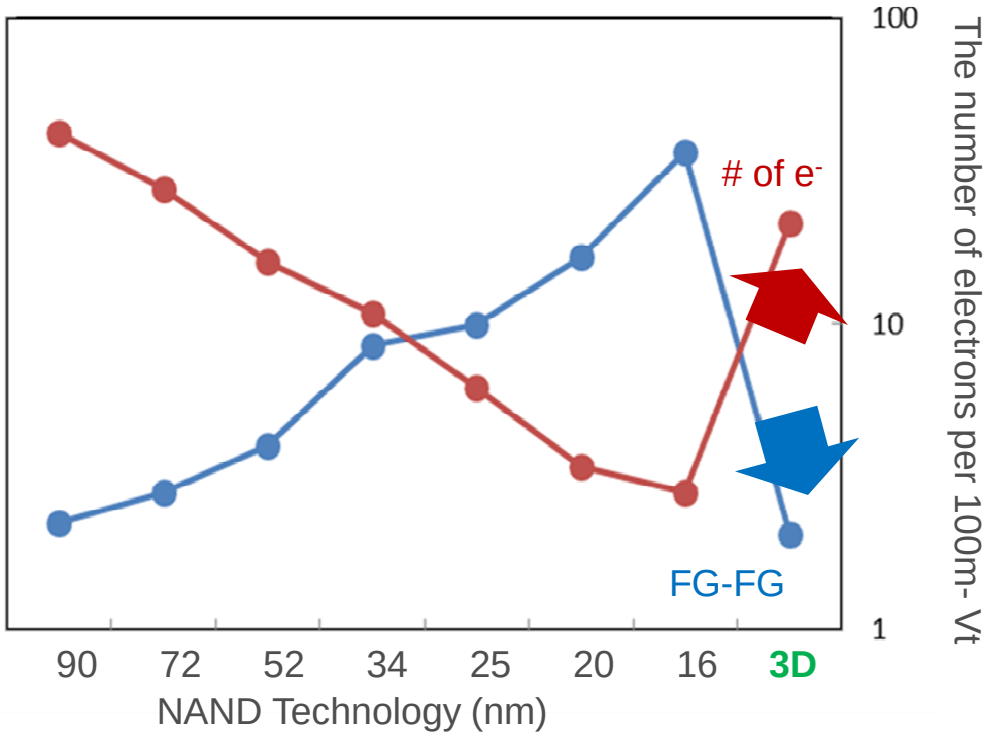


Higher cell CAP: More electrons for a given change in the cell threshold

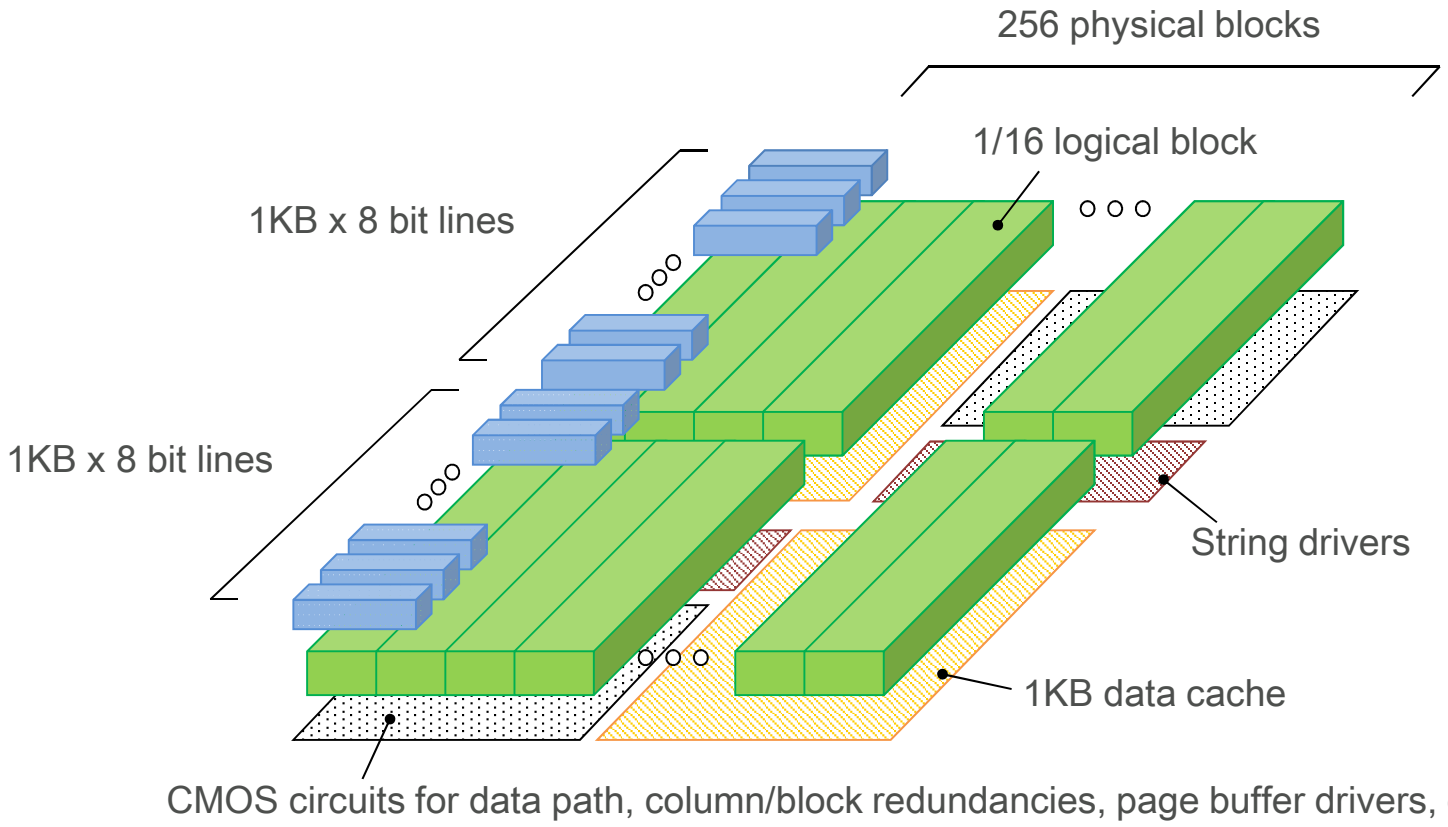
FG NAND reliability

SURROUND GATE : Less interference than 20nm tech





Memory tile with CuA



3D NAND

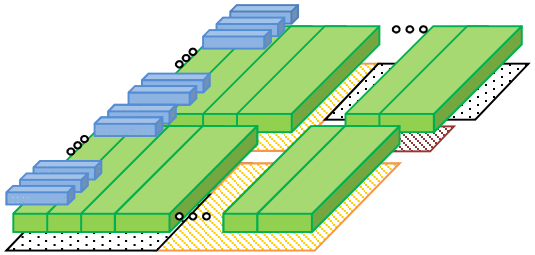
Key advantages

Larger cell size

- Higher cell CAP
  More electrons for a given change in the cell threshold
- Fluctuation effect reduction:
  Reduction on Vt distributions

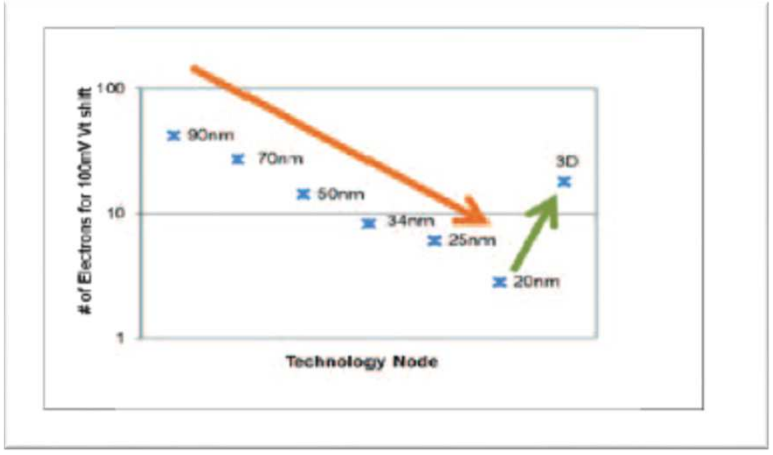
CuA CMOS

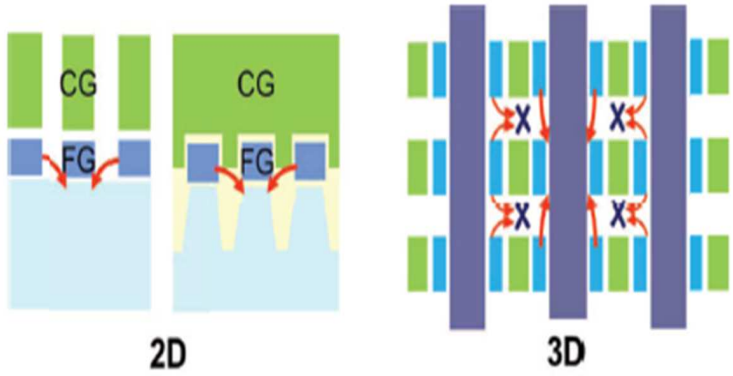
- 2 metal layers above array (bit line power connect)
- 2 metal layer below array



SURROUND GATE

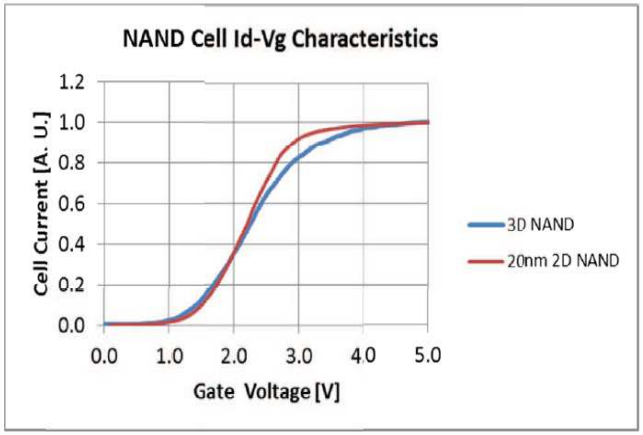
- Less interference than 20nm tech



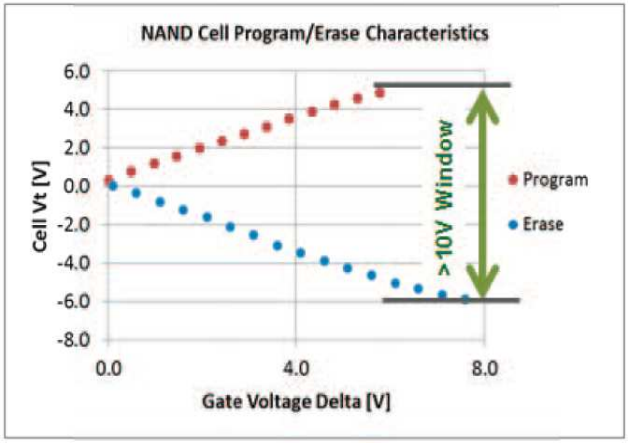


3D NAND
Key Challenges

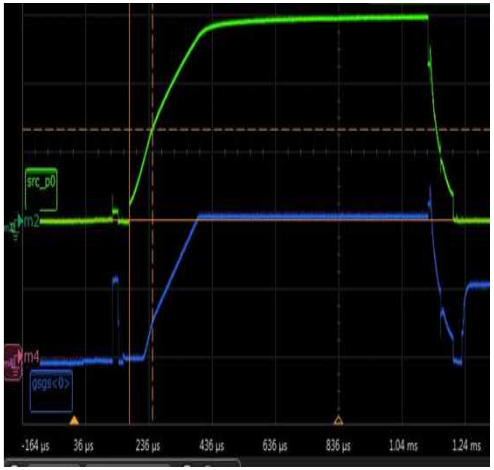
Cell on current



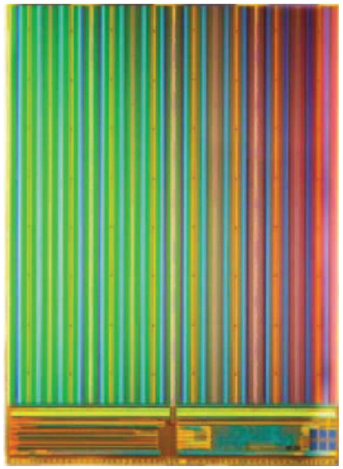
PGM/ERASE Window



Erase GIDL



A 256 2b/cell and 384Gb 3b/cell 3D-Floating-Gate NAND Flash Memory



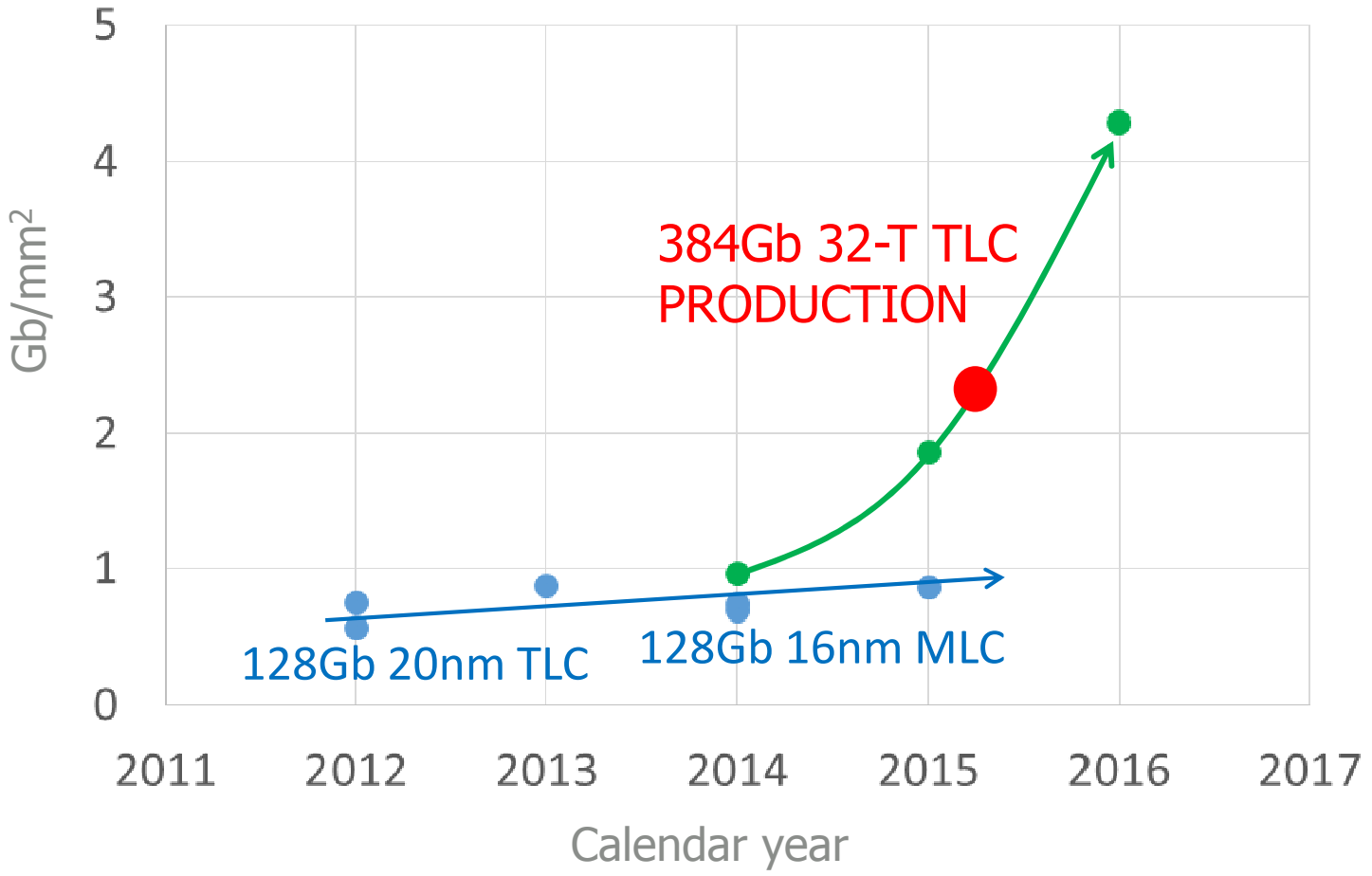
Die Size 168mm^2
2.28Gb/mm2 has been achieved at TLC

Announced in Production Micron – Intel

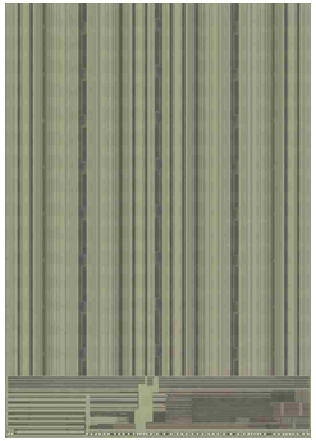
Enables >10TB
in a standard 2.5" SSD

Extends Moore's Law for flash storage

Trend of memory density



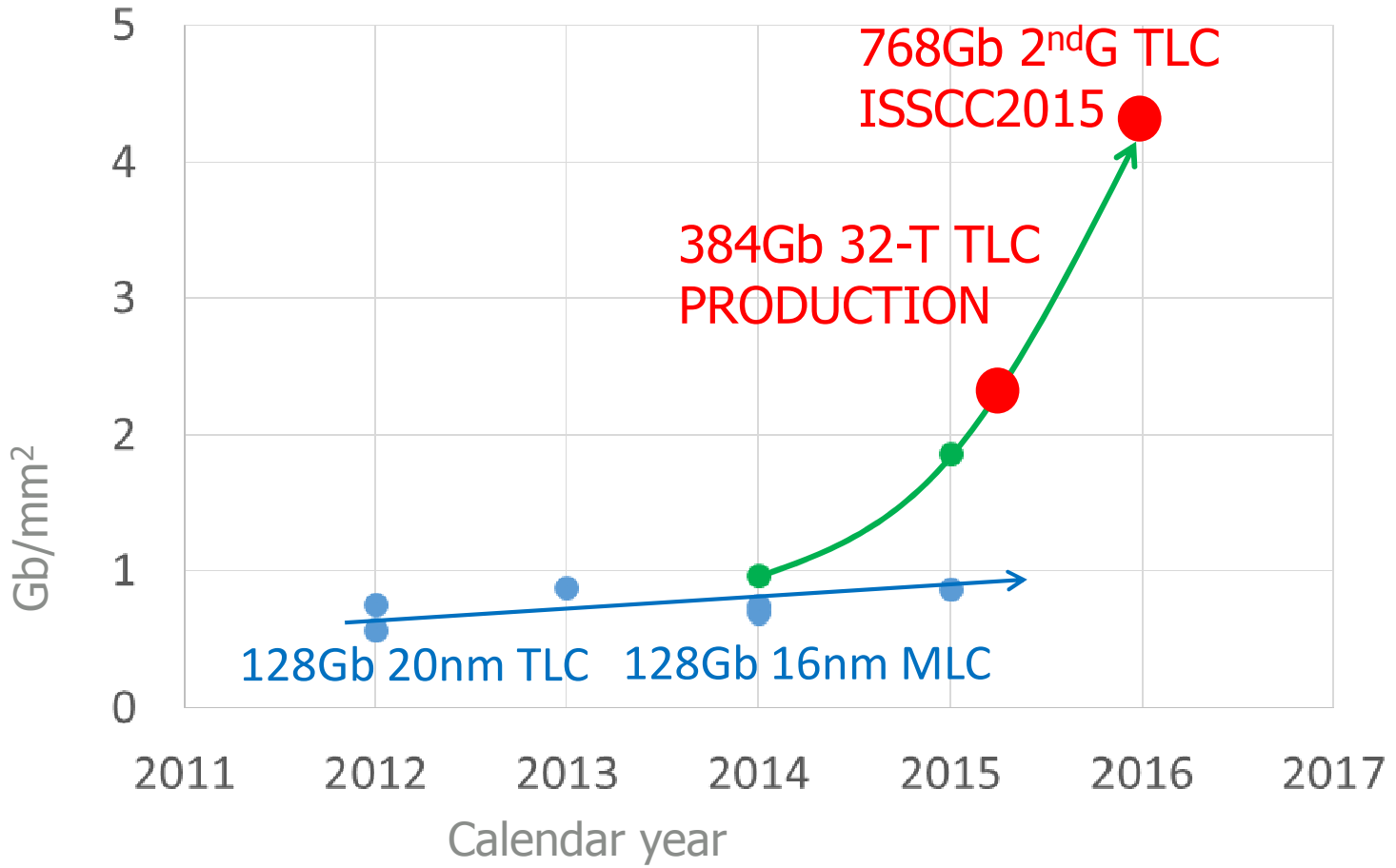
A 512 2b/cell and A768Gb 3b/cell 3D-Floating-Gate NAND Flash Memory



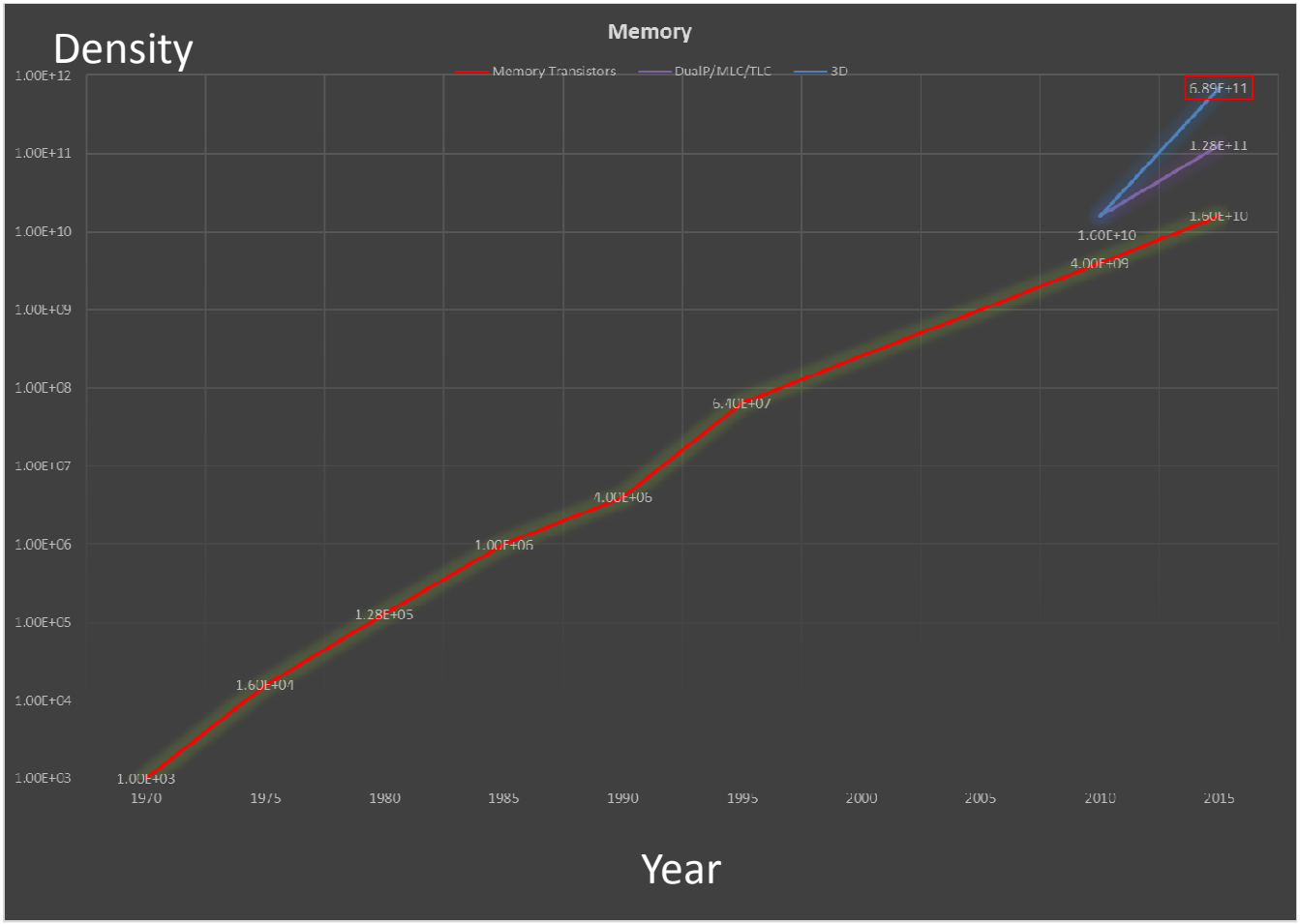
Die Size 179.2mm^2
4.29Gb/mm2 has been achieved at TLC

Announced at ISSCC2016 San Francisco Micron – Intel Feb 2016

Trend of memory density



“Moore’s law” x Memory



3D NAND extends the Moore’s law path for FLASH storage

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